Experiment 12 – Flip-Flops and State Machine Design

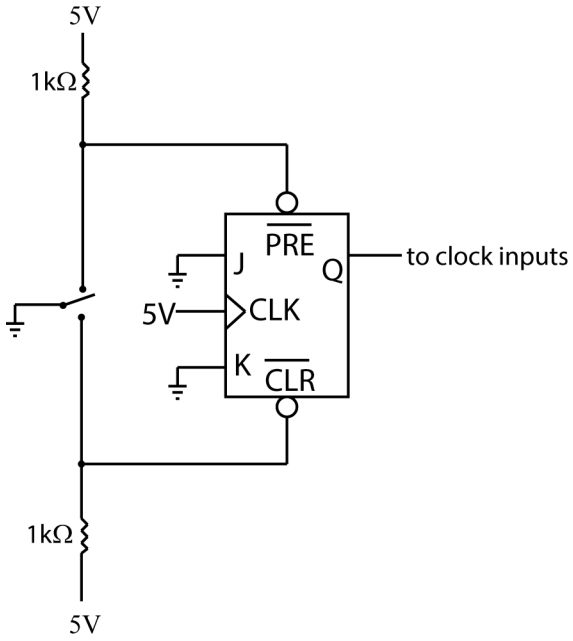
Physics 242 – Electronics

Introduction

Flip-flops are useful in a wide variety of sequential logic circuits, including registers, counters, debouncers, and generalized sequential logic circuits called state machines. In this lab you will use J-K flip-flops to build a state machine that displays the binary count sequence 1 → 2 → 5 → 7 repetitively.

Procedure

Your mission is to design and construct a state machine, or generalized counter circuit, that cycles through the binary sequence 1 → 2 → 5 → 7. Your design should use three J-K flip-flops to represent the three bits needed to represent the numbers, which can be done using two 74LS76 dual J-K flip-flop chips. You may use extra gates (AND, OR, Invert) if you need to. The flip-flops should be clocked synchronously; you will need a debounced switch to use for your clock signal. A debouncer circuit can be constructed conveniently using the remaining J-K flip-flop; the circuit is shown below. The Q output of the debouncer flip-flop is used as the clock input for the other three flip-flops.



Be sure to connect the active-low PRESET and CLEAR inputs to HIGH for your three bits. Use the breadboard LEDs to display your binary count. After you get your circuit working, try using one of the non-debounced breadboard switches to clock your state machine—the results will be instructive.

It will be most convenient for you to design the circuit **before** coming to lab; then the lab period should allow enough time to construct the circuit and get it working. Working circuits should be demonstrated for the instructor. Lab reports should include your design computations, including a transition state diagram, Karnaugh maps for the J-K inputs, the resulting logic expressions, and a neatly drawn schematic of the circuit.

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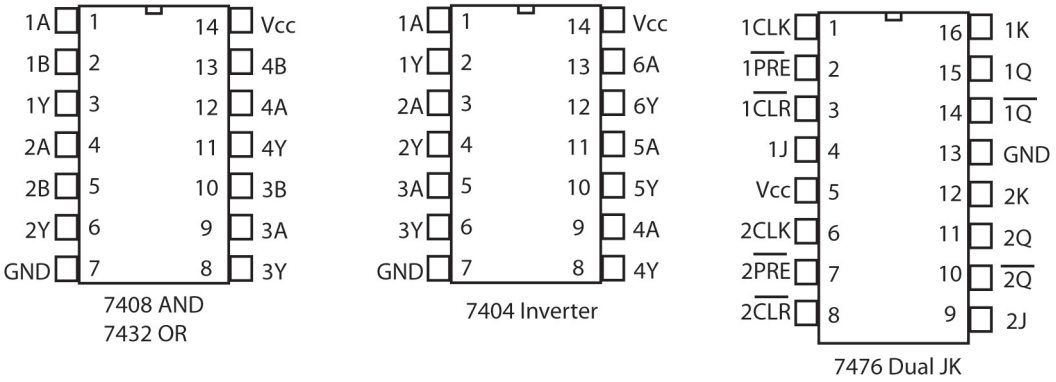

Pin connections for the chips you may need are shown above.